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09/679,461	10/04/2000	Richard J. Ely	2494/103	5412

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/679,461	ELY ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32 and 34-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32 and 34-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 30, 2004 has been entered.

Response to Amendment

2. This Office action is in response to the amendment field on July 30, 2004.

Claim Objections

3. Claims 34-38 are objected to because of the following informalities:

Claims 34-38, line 1, "The apparatus of claim 33, wherein the number of host applications" should be -- The apparatus of claim 32, wherein the number of host applications-- based on the newly filed amendment on July 30, 2004 which indicated claim 33 has been cancelled.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 4-5, 15, 17, 20-21, 31-32, 36-37 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) in view of Peck, Jr. et al. (US PAT. 6,741,258 hereinafter Peck).

Regarding claim 1, Fradette discloses a memory interface device (10, figure 2), i.e., data storage managing apparatus, for interfacing a number of host applications (30, figure 2) to a memory device (20, figure 2) and (col. 3 lines 7-41), the memory interface device comprising a host interface (120, figure 4) for interfacing with number of host applications in a protocol associated with the corresponding host application (col. 3 line 49 through col. 4 line 12 and col. 6 lines 27-51), a memory interface (180, figure 6) for interfacing with the memory device wherein one or more of the host applications and the memory device operate in response to different

protocols (col. 7 line 61 through col. 8 line 5), a number of contexts (124, figure 4) operably coupled to the host interface for receiving memory access requests from the number of host applications (col. 4 lines 18-30 and col. 7 lines 5-17), control logic (60, figure 3) operably coupled to obtain memory access requests from the number of host applications in a protocol associated with the corresponding host interface, translated the memory access requests into memory access requests in accordance with a protocol of the memory device, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications (col. 3 line 45 through col. 4 line 30 and col. 5 line 62 through col. 7 line 28), and provide the result/status information to the number of host applications via the number of contexts in accordance with the protocol associated with each of the number of host applications (col. 9 line 28 through col. 10 line 3). Fradette differs from the claimed invention in not specifically teaches the number of contexts for providing result/status information to the number of host applications based on the receiving memory access requests from the number of host applications, wherein at least one context is provided for each host application. However, Peck teaches a system (10, figure 1) comprising a memory control/interface device (12, figure 1) wherein the interface device comprising a plurality of host interface unit (22, figure 1), and the interface unit for supporting an interface between main memory device (14, figure 1) and a specific processing device, and each of the plurality of host interface unit further comprising a translation look-aside buffer (28, figure 1), i.e., a number of contexts which at least one context is providing for each host application, wherein each of the buffer stores information which is used for translating request from each specific processing device to the memory addresses, respectively, (col. 3 line 44 through col. 4 line 62), in addition,

each of the translation look-aside buffer for executing the requesting from each corresponding processing device and further generate a hit/miss, i.e., result or status, based on the information stores in the buffer (col. 4 line 63 through col. 5 line 10, col. 5 line 37 through col. 6 line 5 and col. 12 lines 42-56). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the interface device of Fradette in having a number of contexts for providing result/status information to the number of host applications based on the receiving memory access requests from the number of host applications, wherein at least one context is provided for each host application, as per teaching by the interface of Peck, because it eliminating the relatively long interconnections which would otherwise be needed to connect multiple processing devices to a single, shared translation look-aside buffer and makes it easier to achieve design timing requirements, and provides a better degree of concurrency is achieved when several processing devices simultaneously issue translation requests.

Regarding claim 4, Fradette discloses the number of contexts comprise a number of context registers sets (126, figure 4) and (col. 4 lines 18-30 and col. 7 lines 5-17).

Regarding claim 5, Fradette discloses each context register set corresponds to one and only one of the number of host applications, i.e., each memory region (126, figure 4) in memory map (124, figure 4) is assigned to a separate interface module (120, figure 4) which corresponding to each host applications (col. col. 4 lines 18-30 and col. 7 lines 5-17).

Regarding claim 15, Fradette discloses the memory interface device as programmed programmable logic device (10, figure 3 and col. 3 lines 21-30).

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 15.

Regarding claim 32, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 36, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 37, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 47, the limitations of the claim are rejected as the same reasons set forth in claim 15.

7. Claims 2, 16, 18, 34 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) and Peck, Jr. et al. (US PAT. 6,741,258 hereinafter Peck), and further in view of Wentka et al. (US PAT. 5,968,114 hereinafter Wentka).

Regarding claim 2, the combination of Fradette and Peck differs from the claimed invention in not specifically teaches the number of host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface. However, Wentka teaches the processing elements (12, figure 1),

comprises 32 separate processing elements 30 and 3 input/output processors (figure 5 lines 65-67), processor interface 50 conforms to a packet processor interface (figure 2, and col. 4 lines 1-6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of the combination of Fradette and Peck in having the host applications comprises a number of packet processing contexts of a packet processor, and wherein the host interface conforms to a packet processor interface, as per teaching of Wentka because it provides to communicate data with the CPU's or processors utilizing the time division multiplexing.

Regarding claim 16, Wentka teaches the memory interface device as an application specific integrated circuit (col. 10 lines 23-28).

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 34, the limitations of the claim are rejected as the same reasons set forth in claim 2.

Regarding claim 48, the limitations of the claim are rejected as the same reasons set forth in claim 16.

8. Claims 3, 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) and Peck, Jr. et al. (US PAT. 6,741,258 hereinafter Peck), and further in view of Bauman et al (US PAT. 5,875,472 hereinafter Bauman).

Regarding claim 3, the combination of Fradette and Peck differs from the claimed invention in not specifically teaches the memory device comprises a content-addressable

memory, and wherein the memory interface conforms to a content-addressable memory. However, Bauman teaches in a multiple processing system comprising a memory interface device (28, figure 2A) for interfacing a number of host applications (31,33,35 and 37, figure 2A) to a memory device (54, figure 2A), the memory interface device comprising a host interface for interfacing with the number of host applications (col. 7 lines 62-64), a memory interface for interfacing with the memory device (col. 9 lines 43-47), and the memory interface further comprising an associated global second-level cache labeled 50 wherein each is mapable to the all of system's addressable memory included in shared main memory (col. 8 lines 3-11 and col. 8 line 57 through col. 9 line 29). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the storage device of the combination of Fradette and Peck is a content-addressable memory, and wherein the memory interface conforms to a content-addressable memory, as per teaching by the computer system of Bauman, because it improves address conflict detection and resolution system for a multiple processor data processing system.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 35, the limitations of the claim are rejected as the same reasons set forth in claim 3.

9. Claims 6-7, 9-10, 12, 22-23, 25-26, 28, 38-39, 41-42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) and Peck, Jr. et al. (US PAT. 6,741,258 hereinafter Peck), and further in view of Hughes (US PAT. 5,784,582).

Regarding claim 6, the combination of Fradette and Peck differs from the claimed invention in not specifically teaches the control logic comprises monitoring logic, scheduling logic, memory interface logic, and result/status logic, wherein the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic, the scheduling logic is operably coupled to schedule memory access operations for the memory access requests, the memory interface logic is operably coupled to generate memory interface signals for interfacing with the memory device over the memory interface, and the result/status logic is operably coupled to provide result/status information to the number of host applications. However, Hughes teaches the control logic comprises monitoring logic (104, 105, 106 and 107 in figure 3), schedule logic (108, figure 3), memory interface logic (111, figure 3), result/status logic (110, figure 3), wherein the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the memory access requests to the scheduling logic (col. 5 lines 37-56), the scheduling logic is operably coupled to schedule memory access operations for the memory access requests (col. 5 lines 63-66), the memory interface logic is operably coupled to generate memory interface signals fro interfacing with the memory device over the memory interface (col. 5 lines 50-54), and the result/status logic is operably coupled to provide result/status information to the number of host applications (col. 5 lines 49-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the control logic of the combination of Fradette and Peck in having monitoring logic, scheduling logic, memory interface logic, and result/status logic, wherein the monitoring logic is operably coupled to monitor the number of contexts for detecting memory access requests and providing the

memory access requests to the scheduling logic, the scheduling logic is operably coupled to schedule memory access operations for the memory access requests, the memory interface logic is operably coupled to generate memory interface signals for interfacing with the memory device over the memory interface, and the result/status logic is operably coupled to provide result/status information to the number of host applications, as per teaching by Hughes, because it provides a greater control over pipeline fullness and reduce the latency.

Regarding claim 7, Fradette discloses each context comprises a context register set (126, figure 4), and wherein the monitoring logic is operably coupled to monitor a predetermined register in each context register set to detect a memory access request (col. 4 lines 18-30 and col. 6 line 27 through col. 7 line 17).

Regarding claim 9, Hughes discloses the memory interface supports pipelining of memory access operations, and wherein the scheduling logic is operably coupled to pipeline a plurality of memory access requests over the memory interface (col. 2 lines 21-31 and col. 5 lines 63-66).

Regarding claim 10, Hughes discloses the scheduling logic is operably coupled to determine that a plurality of memory access requests conflict and execute at least one of the conflicting memory access requests as an atomic operation (col. 2 lines 44-56).

Regarding claim 12, Hughes discloses the result/status logic is operably coupled to correlate result/status information with its corresponding memory access request (col. 5 lines 49-50).

Regarding claim 22, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 23, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 26, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claim 38, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 39, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 41, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 42, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 44, the limitations of the claim are rejected as the same reasons set forth in claim 12.

10. Claims 8, 11, 13-14, 24, 27, 29-30, 40, 43 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) and Peck, Jr. et al. (US PAT.

6,741,258 hereinafter Peck), and Hughes (US PAT. 5,784,582), and further in view of Bauman et al (US PAT. 5,875,472 hereinafter Bauman).

Regarding claim 8, the combination of Fradette, Peck and Hughes differs from the claimed invention in not specifically teaches the predetermined register comprises an instruction register. However, Bauman teaches such (col. 8 lines 43-51). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of the combination of Fradette, Peck and Hughes in having the predetermined register comprises an instruction register, as per teaching of Bauman, because it improves address conflict detection and resolution system for a multiple processor data processing system.

Regarding claim 11, the combination of Fradette, Peck and Hughes differs from the claimed invention in not specifically teaches the scheduling logic is operably coupled to clear the pipeline in order to execute the conflicting memory access request as an atomic operation. However, Bauman teaches such (col. 16 line 42 through col. 17 line 38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of the combination of Fradette, Peck and Hughes in having the scheduling logic is operably coupled to clear the pipeline in order to execute the conflicting memory access request as an atomic operation, as per teaching of Bauman, because it improves address conflict detection and resolution system for a multiple processor data processing system.

Regarding claim 13, the combination of Fradette, Peck and Hughes differs from the claimed invention in not specifically teaches the result/status logic is operably coupled to store the result/status information for each memory access request in a corresponding context. However, Bauman teaches such (col. 9 lines 39-41). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify the computer system of the combination of Fradette, Peck and Hughes in having the result/status logic is operably coupled to store the result/status information for each memory access request in a corresponding context, as per teaching of Bauman, because it improves address conflict detection and resolution system for a multiple processor data processing system.

Regarding claim 14, Bauman discloses each context comprises a validity indicator, and wherein the result/status logic is operably coupled to set the validity indicator in each context when the corresponding memory access is complete and the result/status information is available (col. 22 lines 31-35).

Regarding claim 24, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 29, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 30, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Regarding claim 40, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 43, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 45, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 46, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Response to Arguments

11. Applicant's arguments with respect to claims 1-32 and 34-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hinch (US PAT. 4,642,755) disclosures shared memory with two distinct addressing structures, and wherein digital multi-customer data interface for interconnecting a number of customer terminals to a man packet switching network of a local area data transport system that provides data communication services such as interactive video text service between data service vendors and customers (abstract).

Reynolds et al. (US PAT. 5,590,313) disclosures multiple protocol device interface subsystem and method (abstract).

Jankins et al. (US PAT. 6,272,400) disclosures vacuum network controller includes a host interface for interfacing with a host controller, a component interface for interfacing with vacuum system components (col. 1 line 30 through col. 4 line 14).

Yoshida et al. (US PAT. 6,622,220) disclosures security-enhanced network attached storage device (abstract).

Baker et al. (US PAT. 6,594,735) disclosure a high availability computing system having multiple processing elements capable of simultaneous execution of multiple software programs and seamless software upgrades is disclosed (col. 1 line 58 through col. 2 line 27).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

August 20, 2004

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